Abstract — Photonic integration significantly reduces power consumption, cost, and size while it enhances reliability and functionality. As modern networking and computing systems require high-performance, low-power, and agile optical communications, photonic integration is emerging as critically important technology for future networking and computing. On the other hand, the main challenge with photonic integration lies in the yield and process-compatibility. This paper reviews the impact of photonic integration in optical communications, discusses the challenges, and probes the future prospects for photonic integration.

Keywords — Photonic integration, system on chip,

I. INTRODUCTION

The explosive traffic growth in the Internet is continuing at an accelerating pace even during recent economic downturns. The consumer market has already adopted a massive amount of multi-media communications, video-streaming, and file-transfers on their mobile phones, handhelds, or desktops. Future communication and entertainment services may involve real-time interactive high-definition (HD) video with stereographic or even holographic 3D images. A number of commercial companies have already introduced such systems, and NHK plans to start experimental transmissions of its Ultra-HD broadcast in 2011. With our voice, data, and image transport all converged on the Internet Protocol (IP), the Internet is continuing to see the exponential surge in the communication capacity. Today’s Internet traffic in the United States is estimated at 5 Terabit per second (5 trillion binary digits in one second), and is expected to grow 1000-fold to 5 Petabit per second by year 2015. At the same time, the routers and switches in our central offices supporting such traffic have already grown to be ‘gigantic’!! For example, the highest-capacity (46 Terabit per second switching capacity) commercial routers being sold by CISCO (CRS-1(TM) fully configured) for the core network comes in 1,152 slots of line cards in 80 shelves, consumes nearly a megawatt (0.85 MW), and weighs a ton (56,656 kg). This forces the network operators to equip itself with a large cooling system, and spend ~$1.5 million per year, just for the energy utility cost for operation in a central office (not including capital cost). Even more alarming situations are visible for computing and data center facilities where power consumption is limiting the scalability of such computing/data centers already consuming Megawatts of power. The current situation projects uncertain future as the Internet traffic and computing demands continue to rise exponentially.

Photonic integration offers solutions to many of these issues. The ‘inefficiency’ in today’s communication systems rises mainly from an excessive amount of electronic processing where each bit is stored, processed, and forwarded in high-speed electronics. On the other hand, all-optical pipelined data or signal processing consume nearly no excess energy to serve similar purposes. We have already witnessed the success of this trend in using reconfigurable optical add-drop multiplexers (ROADMs) with smaller IP routers in contrast to using very large IP routers everywhere. Another reason for the ‘inefficiency’ comes from taking optical signals on-chip and off-chip, such that coupling losses will inevitably affect power efficiency. Photonic integration brings the following attractive features compared to conventional approaches involving many (thousands!) discrete modules.

1. Reduced optical power losses: the optical signal stays on-chip all the time until it exits, avoiding power losses at on-chip/off-chip interfaces.

2. Reduced power consumption for cooling: instead of many thermoelectric (TE) coolers used in many packaged chips, a single TE cooler can support a single integrated chip.

3. Reduced packaging and compact size: thousands of discrete packaged modules can be replaced by a single compact packaged integrated chip.

4. Improved Reliability: the reduced number of optical coupling, joints, and packaging also improves reliability.

5. Reduced cost: reduced packaging and handling of individual chips drive the manufacturing cost down.

6. High-performance: the integrated chip can exploit lower loss, higher-speed, and new functionality on the integrated platform to support high-performance.

The photonic integrated circuits (PICs) can potentially spur a similar trend as the great success of electronic integrated circuits as we have seen in the last four decades, where ‘photonic’ Moore’s law may show that the number of integrated photonic components (lasers, switches, etc., instead of transistors) on an integrated circuit (photonic instead
of electronic) double every ~18 months. Recently emerging commercial activities include Infinera’s integrated photonic transmitters and receivers on chip (100 Gb/s commercial at 10 ch x 10 Gb/s, and recently developed 160 ch x 10 Gb/s on 25 GHz grid using passive optics), Luxtera’s silicon CMOS based electronic-photonic integration with InP flip-chip bonding leading to 40 Gb/s active cable (BLAZAR LUX 5010 cable providing 4 x 10 Gb/s multirate connection), and CIPhotonic’s hybrid silica-InP integration supporting quad (4 units) 40 Gb/s optical regenerators on a hybrid chip.

On the other hand, photonic integration can be extremely challenging because the fabrication processes for many discrete devices need to be compatible in the integrated fabrication process flow, and because the yield of the integrated chip must be high enough to support manufacturability and cost-benefits. High-yield and optimized processing is essential. In addition, optimization of an integrated system-on-chip requires optimization of many individual elements at the same time. For instance, photonic integration will require integration of active (lasers, optical amplifiers, switches) elements with passive (waveguides, splitters, couplers) elements, and they all must be optimized for an optimal system performance.

II. NETWORKING AND COMPUTING SYSTEM-ON-A-CHIP VIA PHOTONIC INTEGRATION

This section provides a brief overview of the photonic integration platform developed at UC Davis with partners at Royal Institute of Technology, Sweden, and Multiplex, Inc.

The photonic integration technology developed is meant to solve scalability and energy-efficiency problems related to networking and computing. In networking, IP centric networking propels IP over WDM networking at the core and the edge using optical-label switching, reaching out to secure optical access networks based on IP over optical-CDMA technology. In computing, integrated photonic plane will provide massively parallel optical interconnects between the multiple processor cores and memory units in support of ‘balanced computing’ by matching processing, memory, and communication capacity with distance-independence, ultra-low latency, and concurrency. The most efficient and optimum computing system is a balanced computing system \[1\] capable of providing one byte of memory and one byte per second of memory bandwidth for each instruction per second of computation.

Photonic integration yields future networking and computing systems with extreme power-efficiency and high-performance. Figure 1 shows a schematic of an optical code-division-multiple-access (optical-CDMA) system on a chip capable of supporting ~10 Tb/s local area networking with security enhanced by all-optical codes. The chip contains optical CDMA transmitters and receivers. The transmitter consists of a mode-locked laser (MLL) integrated with a spectral-phase encoder which includes arrayed waveguide gratings (AWGs), amplitude/phase modulators. The receiver consists of a decoder (same construction as the encoder) integrated with an Mach-Zehnder Interferometer (MZI)-based threshold detector (MZI-TD). Figure 2 shows a schematic of an all-optical label switching router on a chip with data plane chip including arrayed waveguide grating routers (AWGRs), MZIs, tunable lasers, and on-chip delays. Figure 3 shows an example of future computing system on a chip using CMOS-compatible silicon photonic integration.
processes. Design-tools are set up in a modular fashion to provide LEGO-like construction of larger systems. The resulting systems provide typically ~1000 times reduction in energy consumption for a given amount of workload (reduced energy-consumption-per-bit).

![Figure 4](image)

**Figure 4. Comparison of conventional electronic IP router cluster with 46 Tb/s switching capacity vs. all-optical label switching router at a similar capacity providing ~2000 reduction in power consumption.**

As an example shown in Figure 4, today’s electronic routers consume relatively large space and power. The state-of-the-art CISCO CRS-1 router with 640 Gb/s capacity (16 slots of 40 Gb/s line cards in one shelf) occupies 213 x 60 x 91 cm³ space, consumes 10.92 kW power, and weighs 723 kg [2]. The multi-shelf configuration of the CRS-1 router can scale up to 46 Tb/s capacity (1,152 slots of 40 Gb/s line cards in 80 shelves (72 linecard shelves and 8 fabric shelves)), consumes 0.86 MW power [3]. All-optical label switching routers have the following opportunities for reducing the size and power consumption.

- Use optical labels at manageable bit rates (e.g. 155 Mb/s ~ 1 Gb/s) while keeping high-speed data (e.g. 40 Gb/s) in the all-optical domain so that the optical label switching router will only keep simple electronics in the control plane and transparent optics in the data plane. (no high-speed electronics necessary).
- Discard the store-and-forward router architecture and adopt the pipelined router architecture to avoid bit-by-bit buffering and processing of data. (no optical RAMs, serial-to-parallel/parallel-to-serial signal processors necessary).
- Exploit further integration and optical interconnects without repeated O/E and E/O conversion steps or on-chip/off-chip coupling stages.

Just from the first two steps above, all-optical label switching routers achieve dramatic reduction in power consumption and size. 1.28 Tb/s capacity optical label switching routers with 32x32 AWGR, 40 Gb/s wavelength converters (2 sets of 32), diode lasers (32 tunable and 32 fixed DFB lasers) [4] and control electronics are expected to consume approximately 128 Watts and occupy 32 x 60 x 32 cm³ space, as opposed to 34 kW, 213 x 120 x 91 cm³ for an electronic counterpart. Monolithic integration [4] of the optical switch fabric, in principle, allows even greater reduction of power consumption down to 14 Watts and physical size to 5 x 5 x 10 cm³. Including all control circuits shown in Figure 2, the power consumption is expected to be less than 200 W for a 46 Tb/s optical label switching router system with integrated photonics.

### III. InP Photonic Integration Processes

This section will show monolithic photonic integration processes using an InP substrate.

![Figure 5](image)

**Figure 5 Cross sectional view of waveguides a) passive waveguide b) phase shifter c) SOA d) laser with FIB facets e) EA.**

![Figure 6](image)

**Figure 6. Traveling-wave phase modulator a) lateral cross section b) longitudinal cross section.**

Figure 5 shows the cross sectional view of the waveguide types in the optical-CDMA [5] and optical-label-switching router devices. The orientation of the cross sections is such that waveguide widths are displayed in the x-direction (lateral), thickness in the y-direction, and the propagation direction of the guided light in the z-direction (longitudinal). Figure 5 (a) displays a passive waveguide of a 500nm thick quaternary Q(1.15) waveguiding (film) layer sandwiched in
InP. Lateral regrown Fe-InP layers passivate the sidewalls of the waveguide and provide electrical isolation. In addition, the lateral regrowth planarizes the waveguide for subsequent metallization steps. Typical waveguide width is 3um, which is a compromise between low propagation loss (2.5dB/cm) and single mode waveguiding (avoiding the symmetrical second order mode). Figure 5 (b) shows a phase shifter, whose refractive index can be changed by injecting carriers in the guiding layer (forward bias), or by applying an electrical field across the Q layer (reverse bias). The metal (AuGeNi/Au) and highly doped InGaAs layer on top provide a low resistance n-contact for electrical connection to an outside current or voltage source, for instance by wire bonding in packaged devices. Semiconductor optical amplifiers (SOA, Figure 5 (c) ) have multi quantum well (MQW) layer on top of the film layer (MQW1). The MQW1 consists of 6 wells of 7nm thick Q(1.25) InGaAsP and 6nm thick InGaAs barriers. The designed gain peak lies at 1550nm. Figure 5 (d) shows a longitudinal cross section of a SOA with etched facets. The focused ion beam (FIB) etched facets provide optical feedback for the SOA and create a laser suitable for integration of the laser with other devices on a single substrate A second type of MQW layer, MQW2 (Figure 5 (e) ) provides a peak gain around 1490nm and has been optimized for electro absorption (EA) modulator operation. For instance for data modulating a pulse train from a 10GHz mode locked laser, or for phase shifting in a MZI structure, as described later in this paper.

Fast code reconfiguration in the optical-CDMA encoder/decoder demands high-frequency (HF) traveling-wave phase modulators. These modulator need to be optimized for low propagation loss of HF electrical fields, velocity matching of the optical group and electrical phase velocity, and maximum overlap between the optical fields and the electrical field.

Figure 6 shows the cross sections of a traveling wave modulator. The most pronounced change with respect to the stack from Figure 5 (a) is the replacement of the n-doped InP substrate with a semi insulating (SI) substrate. The n-contacts are placed on the top side of the chip, on top of an n-InP buffer layer. This configuration reduces electrical propagation loss by reducing the amount of electrical field in n-doped layers. A benzocyclobutene (BCB) layer on both sides of the Fe-InP provides additional support for the metal contact layer on top. The SiO$_2$ layers provide an electrically isolated cohesion layer for the metal. Removal of the n-buffer layer between adjacent modulators isolates their n-contacts.

The epitaxy on a SI substrate consists of a 500nm thick n-InP buffer layer, a 500nm Q(1.15) layer, a 2.0 um p-InP layer with gradually increasing p-doping towards the top, and a 100nm think InGaAs contact layer. A RIE etch through the Q layer defines the waveguides. A lateral Fe-InP regrowth passivates the waveguides and planarizes the surface. In order to reduce the overlap of the electrical field with the laterally regrown Fe-InP, a wet chemical etch reduces the Fe-InP width to 4um on both sides, which is wide enough not to affect the optical guiding properties of the waveguide. Furthermore, since the microwave electrical field tends to have a lower propagation velocity compared to the optical field, increasing the electrical field confinement in air (by thinner Fe-InP) improves velocity matching. The etching stops at the top of the n-buffer layer to enable the n-contacts.

Figure 5b shows the same modulator, but in a longitudinal cross section through the waveguide center. The segmentation of the p-contact geometry provides velocity matching of the electrical phase with the optical group velocity. The segmentation consists of ion-implantation to locally destroy the conductance of the p-layer and a BCB layer to avoid metal-semiconductor contact on the ion implanted segments.

IV. InP PHOTONIC INTEGRATION COMPONENTS

A SPECTS O-CDMA system employs spectral encoding of ultra-short optical pulses from a mode-locked laser for data transmission. Spectral coding in the transmitter spreads pulses in time at expense of peak power. The decoder only reconstructs the ultra-short, high peak-power pulse if the encoder code and decoder code are conjugates of each other. (The decoder and encoder are similar devices.) The receiver, after the decoder, discriminates correctly decoded pulses from incorrectly decoded pulses by nonlinear threshold detection. The receiver detects a “1” bit only if a pulse has sufficient peak power (correctly decoded). Otherwise, the receiver detects a “0” bit for a time-spread pulse. The following sections elaborate our results with these InP based OCDMA components.

A. Mode-locked laser

An ultrafast light source based on semiconductor mode-locked (ML) laser is required for as transmitter in an Optical-CDMA integrated photonic circuit. We have developed a 10 GHz colliding-pulse mode-locked laser (CPM) [8-9] in the platform from Figure 1, allowing for the monolithic integration of the CPM laser with other O-CDMA elements discussed in the rest of the paper. Compared to a regular mode-locked laser design, the CPM laser operates in the configuration where two symmetrically counter-propagating pulses collide and bleach the saturable absorber
located at the center of the laser cavity, resulting in deeper saturation and more stable mode locking.

Figure 7. SEM image of a 10 GHz CPM laser with integrated active-passive waveguides.

Figure 7 shows the SEM image of a fabricated CPM laser. The required CPM cavity length for 10 GHz operation exceeds 8 mm, which for all all-active design will require fairly high drive current. Furthermore, long (>4 mm) all active mode ML lasers for achieving lower repetition rate tend to suffer from strong pulse shaping effects, resulting in poor chirping and jitter performance [10]. Adopting the active-passive integration process in Figure 5 allows for reducing the active section length to minimizing these effects and the drive current requirement [8]. The active-passive interfaces are designed to be laterally tilted at 45 deg relative to the waveguide direction. This lateral tilt is critical for eliminating unwanted secondary pulses originating from residual reflections at the interfaces, resulting in much improved mode locking performance compared to the unilted designs. The active region has total length of 2000 μm, dividing into two gain sections and sandwiching the 45 μm wide saturable absorber (SA) located at the center. The waveguide is further extended symmetrically on both sides with passive sections, forming the 8200 μm long laser cavity.

The CPM laser can be synchronized to an external system clock through either electrical hybrid mode locking (HML) [10-11] at the fundamental or a subharmonic frequency, or through the optical synchronous mode locking (OSML) approach [12-13]. In the electrical HML configuration, RF modulation signal is applied to the saturable absorber of the CPM laser through a Ground-Signal-Ground microwave probe, while the two gain sections and the SA are DC biased through DC needle probes (forward current injection) and the microwave probe (reverse bias voltage) through a bias-tee connection respectively. We have previously reported in detail the electrical HML investigation of the 10 GHz CPM laser [8]. By applying the RF clock signal matching the passive ML frequency of 10.3 GHz at 19 dBm, we obtained nearly transformed limited output with pulse width of 1.75 ps and time-bandwidth product 0.33, with relatively low timing jitter. This short pulse, low chirp performance can be attributed to the careful balancing of the pulse broadening and chirping effects inside the relatively short gain sections and the SA pulse truncating effects respectively [15]. Minimizing the active-passive interfacial reflections also plays an important role for achieving optimal pulse quality.

For synchronizing remote photonic chip based system nodes in an O-CDMA network, the electrical HML approach, while relatively easy to implement on a single device, requires supplying system clock signal at relatively high RF power to multiple distant locations, and expensive to implement. The alternative OSML approach, would involve the simple routing of a single optical clock signals through the network fiber for injecting locking of all CPM laser sources simultaneously.

For OSML optical injection locking characterization, a commercial tunable mode-locked fiber laser synchronized to an RF synthesizer clock source provides the optical clock, which is coupled into the 10 GHz CPM laser through a polarization-maintaining (PM) attenuator and a lensed fiber. The CPM output, collected through a lensed fiber from the other output facet, passes through a 3 nm tunable filter for removing any residuals of the injection signal, and then routes to different instruments for time and frequency domain measurements, and the Bit-Error-Rate-Tester (BERT) for BER measurements.

Figure 8 (a) shows the RF power spectra of a 10 GHz CPM laser under both passive ML and optical injection locking conditions. Also sampling scope traces of the CPM laser output triggered with the RF clock source under (a) passive (b) optical injection locking conditions.

Figure 8 (a) shows the RF power spectra of a 10 GHz CPM laser under both passive ML and injection locking conditions at -10 dBm coupled optical power, with the injection signal at 1546 nm, 8 nm negatively detuned from the passive ML wavelength. Figure 8 (b) shows the corresponding 50 GHz optical sampling scope traces, triggered with the RF synthesizer clock. Compared to passive mode-locking the RF spectral lineshape narrows significantly in Figure 8 (a) under optical injection, corresponding to the sharply reduced timing jitter after synchronization. The estimated RMS timing jitter of the injection-locked CPM laser is 0.5 ps by integrating the single-side-band (SSB) phase noise spectrum, while the injected laser clock signal has RMS jitter of 0.17 ps. The effect of optical injection is primarily phase synchronization, without any
observed changes in the pulse width and spectrum of the CPM laser output. Optical phase synchronization effects can be observed at injection power level as low as -23 dBm. BER measurements also demonstrated that the CPM output is error free with BER<10^-11 under PRBS 2^{23}-1 data modulation, demonstrating that optical injection locked 10 GHz CPM laser can indeed serve as a viable short pulse light source in O-CDMA and other photonic integrated circuit applications.

B. InP Encoder and Decoder

Previous integrated O-CDMA encoders are either based on silica arrayed-waveguide gratings (AWG) with non-programmable external phase shifters [16] or based on ring micro-resonators with relatively slow heater based phase shifters [17]. On the other hand, InP platform based SPECTS O-CDMA (Fig. 1) encoders and decoders offer rapid code reconfiguration by employing electro-optical phase shifters and the possibility of realizing monolithically integrated O-CDMA transmitters and receivers [5].

![Figure 8](image8.png)

Fig. 8. Integrated O-CDMA transceiver chip containing Transmitter (Trx) and Receiver (Rcv) sections. Both Trx and Rcv include O-CDMA encoder/decoder consisting of AWGs and phase modulators.

Figure 8 shows the fabricated O-CDMA transceiver. The AWG pair performs spectral de-multiplexing and multiplexing. Phase modulators in between the AWGs apply a phase shift, corresponding to the desired O-CDMA code, to each de-multiplexed spectral channel. The input and output waveguides of the device are selected for optimal wavelength match of the two AWGs. Figure 9 shows the packaged chip with electrical and optical interfaces.

![Figure 9](image9.png)

Figure 9 Packaged O-CDMA transmitter chip with fiber pigtails.

Figure 10 displays the effect of MUI on the pulse output. Figure 10 a shows the cross-correlation trace after the encoder-decoder pair with phase error compensation but without coding. The ~3ps time-gating around t = 0ps (dotted line) removes the ringing peaks at the expense of signal power. Figure 10 b shows the cross-correlation trace of the output of the encoder-decoder pair without interferers (extra users), with W1 and W1* codes for encoder and decoder for 2 time slots. Figure 10 (c) and (d) show the traces with added interferer W2 and interferers W2 and W4, respectively (two time slots).

Figure 11(a) shows the BER measurement results for the 6-user OCDMA system with InP encoder and decoder. Back-to-back data were taken with the O-CDMA encoder and decoder pair bypassed. Received power in all BER curves is defined as the average input power per user as measured at the input of the “O-CDMA receiver”. The 2-user and 4-user experiments demonstrated error-free operation and a power penalty of 5.5 dB at BER = 10^-9 with respect to back-to-back. The penalty can be mainly attributed to power lost to the ringing peaks. The 6-user case attained an error floor at 10^-9, primarily due to MUI inside the time gate. MUI effects are relatively small for 2 and 4 users, resulting in no observable noise floor. For a narrower time gate window and/or longer code
length would mitigate the MUI effects significantly and an error-free operation is expected.

In order to investigate the effect of the spectral filtering and loss in the InP based en/decoders, we repeated the BER measurement but replaced the InP devices with SLM based en/decoders. SLM devices approach ideal coding performance due to their rectangular filter shape. Figure 11 (b) shows the BER measurement result and eye diagrams. The 2-user and 4-user experiments demonstrated error-free operation with a power penalty of 2 dB and 5 dB, respectively, at BER = 10^-9. The error floor below 10^-9 for the 6-user SLM case confirms that MUI and not the InP chip response is the dominant limitation for error-free operation of O-CDMA system.

**C. MZI threshold detector development**

The last step of the SPECT-OCDMA transmission link requires non-linear optical thresholding: the detection of properly decoded optical pulses with narrow pulse width and high peak power, and the blocking of the time spread improperly decoded interferer signal. Compared to other nonlinear fiber based thresholder approaches, The MZI thresholder is less bulky, more sensitive [22-23] and is compatible with monolithic integration with other semiconductor components. Here we describe an improved “clock-gated” MZI scheme with respect to the “self-gated” approach reported previously [5]. Both schemes depend on differential operation of the MZI.

Figure 12 shows the self-gated and clock-gated MZI operation. In the self-gated scheme, no external clock signal is provided. The decoded pulse is split in two and each part enters a distinct MZI arm with a time delay. Only the correctly decoded pulses have sufficiently fast rising edges to saturate the non-linear optical elements in the MZI arms, opening a differential gate for the CW probe signal. The clock-gated scheme uses the external short pulse clock signal for generating the differential gate of the MZI.

For improved performance, we investigated a new class of integrated MZI, based on reverse biased electro-absorbers (EA) [24] rather than SOA based MZIs. The reverse biased EA sections result in faster carrier sweep out (tens of ps) and less Amplified Stimulated Emission (ASE) noise compared to the conventional forward biased SOAs in the MZI arms, favoring high speed, lower power consumption operation with greater cascadability.

**Figure 13.** a) Photograph of fabricated EA-MZI with active-passive integrated waveguide. b) Normalized MZI transmission vs. pump input power, (inset) showing EA-MZI output at 2.5Gb/s.

Figure 13 a) shows the fabricated EA-MZI with four multi-mode interference (MMI) based 3 dB couplers, two active EA sections of 200 um and 50 um in length and two 600 um long phase shifters. The phase modulators allow the MZI to be biased for optimal destructive interference at the MZI output, whereas the unequal EA section lengths allow better power balance between the two arms.
(without pump). Injection of an optical pump signal into the shortest EA induces cross phase and amplitude modulation, and the device operates as a ‘non-inverting’ optical switch (or wavelength converter).

Figure 13b shows the normalized MZI switching output vs. pump input power with the pump signal at 1540 nm, probe signal at 1550 nm, and the upper and lower EA reverse biased at -1 V and -12 V respectively. A 10 dB pump power change (ER) resulted in 18 dB output switching ratio, demonstrating the optical signal regeneration capability of the EA-MZI. Figure 13b inset shows the MZI wavelength conversion output from a 2.5 Gb/s 2¹-1 pseudo-random-bit-sequence pump input. These results demonstrate the optical switching capacity of the EA-MZI device, and its potential as a high speed, low power, and low noise optical thresholder element.

D. CMOS-compatible Silicon-based Switches/Demuxes/Routers

Integrated silicon photonic fabrication processes included standard silicon CMOS fabrication processes. Figure 14 (a) shows a top-view scanning electron microscope (SEM) image of a fabricated single microring resonator. The microring resonator radius is 10 µm. The waveguide width is ~0.45 µm and the height is ~0.2 µm with a ~40 nm silicon layer left as the slab region. The gap between the waveguide and microring resonator is 0.25 µm. Figure 14 (b) shows the waveguide cross-section before oxide deposition. Slight roughness in the waveguide sidewall is visible. Figure 14 (c) shows the waveguide cross-section after oxide deposition (~0.7 µm thick). Subsequent dicing of the wafer into mm-sized dies and polishing of the die facets prepared the die for high-quality optical coupling.

The device transmission spectra measurement employed an external-cavity wavelength-tunable diode laser (1524 nm–1576 nm, ~300 kHz linewidth) as the light source. The input laser beam was first pre-amplified by an erbium doped fiber amplifier (EDFA) to ~16 dBm optical power to compensate for the device insertion loss (~20 dB). We used a polarization controller to set the polarization to TE polarization (electric field parallel to the chip). The input light was butt-coupled to the device through a tapered single-mode silica fiber. The tapered fiber has a spot size of ~2.5 µm. The input waveguides of the devices are also laterally tapered to ~2.5 µm to reduce coupling loss. At the output, we used an objective lens with numerical aperture NA = 0.65 to collect the output light. The collected light was finally detected by an InGaAs photodiode detector.

Figure 15 (a) Microscope top view of the fabricated crossbar basic building block, (b) measured transmission spectra for the device in (a), (c) microscope top view of the fabricated 3×3 crossbar, (d) measured transmission spectra of the device in (c), (e) microscope top view of the fabricated 4×4 crossbar, (f) measured transmission spectra of the device in (e).

Figure 15 (a) and (b) show the crossbar basic building block microscope image and its measured through and drop transmission spectra. The resonance free spectral range (FSR) is ~14 nm and the resonance bandwidth is ~1.6 nm (200 GHz). Figure 15 (c) and 6(d) show the fabricated 3×3 crossbar and the corresponding measured spectra for its three output ports. The resonance wavelengths of the three resonators are separated by ~75 GHz. As predicted by the modelling, when the resonance bandwidth is larger than the channel spacing, strong interference occurs among resonators, and consequently the drop transmission spectra (O₁ and O₂) exhibit less pronounced peaks. These weakened drop peaks deteriorate optical signal transmission. Figure 15(e) shows the fabricated 4×4 crossbar using the SOI wafers with a device layer thickness of 0.26 µm. Figure 15 (f) shows the corresponding measured spectra for its four output ports. As the light transmission goes through more stages, cross interference between different resonators is more significant, which increases the channel crosstalk. Fabrication induced phase error in the microring resonators can cause resonance shift from the desired values. In order to compensate for this error, post-fabrication trimming techniques, such as electron beam trimming [6], can be used to accurately control the resonance wavelengths. Alternatively, doping the desired waveguide regions using ion implantation techniques is also able to change the refractive index [7].
We characterized the 3×3 crossbar dynamic performance by measuring the transmission bit error rate (BER) at 10 Gbit/s and 40 Gbit/s data rates. The pseudo-random binary sequence (PRBS) used for the 10 Gbit/s measurement was $2^{31}$-1 bits long, and $2^{31}$-1 bits long for the 40 Gbit/s measurement. Figure 16 shows the setup for the BER measurement. 10 and 40 Gbit/s NRZ-OOK optical signals were generated by modulating an input laser beam using a Lithium Niobate (LiNbO$_3$) Mach-Zehnder modulator driven by a pulse pattern generator (PPG) at 10 and 40 GHz. The modulated signal was then amplified by an EDFA (saturated at 16 dBm optical power) before coupling into the chip. The transmitted signal was post-amplified by another EDFA (saturated at 16 dBm optical power) and then passed through a tunable band pass filter (BPF). The optical signal was finally converted to an electrical RF signal using a high speed photodetector, and analyzed by a bit error rate tester (BERT), which is synchronized to the PPG.

We tuned the laser wavelength to the resonance wavelengths (near 1550 nm) for O$_1$ and O$_2$ BER measurements and a non-resonance wavelength (near 1543 nm) for the O$_3$ BER measurement. Figure 16 (a) and (b) show the BER test results for all three output ports and back-to-back (BtB) transmission at 10 Gbit/s and 40 Gbit/s. The power penalty for O$_3$ is smaller than that for O$_1$ and O$_2$ as expected, since the signal coming out of O$_3$ travels through the crossbar without experiencing any resonance. The power penalties for the drop channels are slightly higher, resulting from the limited resonance bandwidth and interference induced resonance line-shape distortion (Figure 15 (d)) [8, 9].

V. SUMMARY

This paper discussed the impacts of photonic integration in networking and computing systems, and demonstrated the actual photonic integrated system-on-a-chip using InP and silicon platforms. The impacts in terms of reduced power consumption and size, and improved reliability and functionality are significant. Overcoming challenges by improving yield would be a key to realizing future networking and computing systems-on-a-chip.

ACKNOWLEDGMENTS

The author would like to thank the members of next generation networking and systems group at UCDavis and their collaborators around the world who contributed to this paper. The author wishes to acknowledge support by DARPA NGI Initiative F30602-98-C-0216, DARPA and SPAWAR under agreement N66001-01-1 and under Contract HR0011-04-1-0054 and F30602-00-2-0543, and by the National Science Foundation under grant number ANI-998665, NRT-0335301, NETS-0435529.

REFERENCES