A 10-Gbps BM-CDR Circuit with Synchronous Data Output for Optical Networks

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Abstract—This letter presents a 10-Gbps burst-mode clock and data recovery (BM-CDR) circuit based on an analog phase-picking method. The experiment demonstrates that the proposed BM-CDR circuit is able to align the BM data to a local clock with a phase alignment accuracy of ±π/4, a 25-ns latency and zero bit loss. The circuit further resamples the aligned data using the local clock for jitter reduction. The experiment shows error-free operation of the BM-CDR circuit for burst-mode data packets with various phase delays.

Index Terms—Burst mode, clock and data recovery, bit synchronization, multiphase clock

I. INTRODUCTION

The rapid growth of cloud computing, data centers [1], and passive optical networks (PONs) [2] is driving the needs for viable burst-mode receiver technologies at high data rates [3]. The burst-mode receiver (BM-Rx) plays an important role in amplitude and phase recovery at the beginning of the data packet. Fig. 1 shows a generic schematic of a BM-Rx. At the front end of the BM-Rx is a burst-mode limiting amplifier (BM-LA) with automatic gain control (AGC) and automatic threshold control (ATC). The BM-CDR circuit conducts fast clock and data recovery (CDR) together with phase acquisition. This Letter discusses the BM-CDR aspect of the BM-Rx operating at 10 Gbps. There have been numerous BM-CMR studies. Reference [4] incorporates gated voltage controlled oscillators to acquire rapid phase locking, but results in higher phase noise and undesired jitter and intersymbol interference (ISI). The conventional injection locking technique [5] suffers from process, voltage and temperature variations. Oversampling used in [6] can be impractical at data rates beyond 10 Gbps. On the other hand, oversampling by multi-phase clocks only requires components operating at a frequency equal to the bit rate. In addition, this method can provide seamless and stable local clock output desirable for many signal processing and communication systems involving field programmable gate array (FPGA) and application specific integrated circuits (ASICs)[7]. This Letter proposes and demonstrates a BM-CDR technique employing an analog phase picking method which aligns the data packets to a local clock based on the phase difference between the extracted clock and four phase-delayed copies of the local clock. The aligned data packets are further re-sampled by a D-type flip-flop (DFF) triggered by the local clock for jitter reduction. The experimental prototype BM-CDR Circuit achieves a phase alignment accuracy of ±π/4 and a 25-ns latency at 10 Gbps without losing any bits. This meets the need of future 10 gigabit Ethernet PON (10G-EPON) applications (IEEE802.3av 10G-EPON standards) and future data center networks.

Fig. 1. Generic schematic of a BM-Rx. (PD: photo-detector; TIA: transimpedance amplifier; BM-LA: burst-mode limiting amplifier; AGC: automatic gain control; ATC: automatic threshold control)

II. BM-CDR CIRCUIT IMPLEMENTATION

A. Circuit description

Fig. 2 shows the proposed BM-CDR circuit block diagram implemented for operating at 10 Gbps for a non-return-to-zero (NRZ) data packet stream. The main building blocks include a custom designed high-speed printed circuit board (PCB) and an Atlys Spartan-3 FPGA development board. The incoming optical data is O/E converted and split into two copies. One copy is delayed and split into four phase-adjusted copies which enter a 4:1 selector. The other copy of the incoming data enters an NRZ-to-RZ converter followed by a band-pass filter (BPF) with a Q of 200 for clock extraction [8]. The extracted clock is then amplified and phase delayed before entering the RF mixers to frequency mix with the four copies of the local clock for phase detection. The threshold of the four comparators is set to 60 mV based on the maximum mixer output voltage in the worst case as described in Fig. 3 and Fig. 5. By matching the mixer outputs to a look-up table, the FPGA selects one of the four phase-shifted packets at the selector inputs as the optimum recovered data and feeds it to a DFF for data retiming. Retimed data is then sent to the next stage for further data processing.

The multiphase clock and data generation is achieved by the
1:4 fanout and the electrical coplanar waveguide with ground plane (CPWG) on the PCB. The measured delay deviations from the target values are within ±2ps, which is reasonable considering the skew value (±3ps) specified in the 1:4 fanout (HMC940LC4B) datasheet. Fig. 4 and Fig. 5 show four phase-delayed copies of the data and the measured four mixer outputs as functions of applied phase delay to the data respectively. The evenly spaced curves indicate well-controlled CPWG delay lines.

![Block diagram of the proposed 10-Gbps BM-CDR circuit](image)

**Fig. 2.** Block diagram of the proposed 10-Gbps BM-CDR circuit. (O/E: optical to electrical converter; LA: limiting amplifier; AMP: amplifier; BPF: bandpass filter; LO: local oscillator)

**B. Phase alignment accuracy analysis**

The phase delay between the extracted clock and the local clock can be uniquely identified by frequency mixing the extracted clock with two phase delayed copies of the local clock [9]. But low speed (<1GSps) analog-to-digital converters (ADC) used to digitize the mixer outputs would introduce significant conversion latency. So there is a trade-off between cost, resolution and latency. Here, the prototype employs four comparators with a maximum toggle rate of 3.84 Gbps, which are equivalent to a 2-bit ADC. The phase alignment accuracy of this configuration can be expressed as

\[
S = \frac{\pm \pi}{n}
\]

where \(n\) is the number of mixers used. The largest misalignment (\(\pi/4\)) happens when two adjacent mixers have the same output voltages as in Fig. 3(b), where \(n = 4\). Either path can be selected by the FPGA to align the burst-mode data to the local clock.

![Mixer output as a function of phase difference between the two mixer inputs](image)

**Fig. 3.** Mixer output as a function of phase difference between the two mixer inputs (a) best case (b) worst case.

The experimental setup of Fig. 6 emulates and generates burst-mode data packets with varying phases to evaluate the performance of the BM-CDR circuit. The pulse pattern generator (PPG) generates a periodic 1024-bit long sequence (constructed by \(2^4-1\) PRBS sequence) followed by a 1546-bit long guard time. The electrical signal is amplified and fed into a 10-Gbps optical intensity modulator (IM) to modulate the output of a tunable laser diode (TLD) at 1545 nm. The modulated optical signal is amplified and split into two copies by a 50:50 fiber splitter. After proper delay adjustment, the optical signals in the two branches are interleaved by another 50:50 fiber coupler. In the end, the interleaved signal is O/E converted and sent to the proposed BM-CDR circuit.

The minimum latency introduced due to phase acquisition is approximately 25 ns in the current configuration, and is determined mainly by the combined sum of the settling time of the mixer output at the beginning of the data packets (~20 ns when using a BPF with a \(Q\) of 200), the FPGA decision time (4ns), and the 4:1 selector select time (< 100ps). The mixer output settling time depends on the \(Q\) of the BPF used to extract the data clock. A BPF with a lower \(Q\) can be used to reduce the settling time, but at the price of larger pattern dependence (the mixer output level is more sensitive to the zero bits in the data packets). A BPF with a \(Q\) of 200 is used...
for this particular application, which results in a reasonable mixer settling time of 20 ns at the beginning of every packet and a stable output with ±3 mV fluctuation across the entire packet duration. Fig. 7 shows the output waveforms of the extracted clock and the local reference clock demonstrating no significant jitter or degradations during the clock extraction.

![Waveform](image_url)

**Fig. 7.** Output waveforms of (a) reference clock and (b) extracted clock recorded on Agilent 86100A where rms jitter is measured and recorded.

Fig. 8 shows the scope traces of the four mixer outputs for the interleaved packets. Measurements show the mixer outputs are able to stabilize within 20 ns from the beginning of each packet. The FPGA is programmed in such a way that it only reads the comparator results and reconfigures the selector after the mixer outputs stabilize. A counter implemented in the FPGA filters out the short spikes in the mixer outputs at the end of each packet. As shown in Fig. 8(a), setting the minimum packet guard time to 5 ns results in proper responses from the mixer outputs as in Fig. 8(b) and (c), with the phase difference between consecutive packets set at \( \pi/4 \) and \( \pi/2 \) respectively. Fig. 8(d) shows the case with the guard time set to 500 ps and the phase difference > \( \pi/2 \). In this case, the mixer is still able to track the phase changes between adjacent packets, but the FPGA triggered by a 500-MHz clock is not able to properly align the selector control signals with the phase delayed packets at the 4:1 selector inputs. In the rest of the measurements, the guard time between packets is kept above 5 ns, although future FPGA or ASIC based BM-CDR circuit should be able to support < 1 ns guard time. During longer guard times, all the mixer outputs go to 0 V which is below the 60-mV threshold used in the experiment. As a result, the FPGA will not be triggered and the configuration of the 4:1 selector will remain the same. No additional circuit components are used for burst envelope detection.

![Scope traces](image_url)

**Fig. 8.** Scope traces of (a) the incoming data packets with a minimum guard time of ~5 ns, (b) corresponding mixer outputs when the phase difference between the two packets is ~\( \pi/4 \), (c) corresponding mixer outputs when the phase difference between the two packets is ~\( \pi/2 \), (d) corresponding mixer outputs when the phase difference between the two packets is > \( \pi/2 \) and the guard time is ~500 ps. Comparator threshold is set to 60 mV.

Fig. 9 shows the data eye opening before the DFF as a function of the TDL settings in Fig. 6. The measurement data matches the theoretical estimation well. In the theoretical estimation, the maximum eye opening is set to 75 ps which is the measured data eye opening when synchronous data packets are sent to the circuit. The deviation is mostly due to the output skew of the 1:4 fanout and the noise in the circuit.

![Eye opening](image_url)

**Fig. 9.** Data eye opening before the DFF as a function of the TDL settings in Fig. 6. The measurement data matches the theoretical estimation well. In the theoretical estimation, the maximum eye opening is set to 75 ps which is the measured data eye opening when synchronous data packets are sent to the circuit. The deviation is mostly due to the output skew of the 1:4 fanout and the noise in the circuit. During the bit error rate (BER) measurement, the guard time between the adjacent packets (gap 1 and gap 2 in Fig. 6) are set to 23.5 ns (235 bits) and 27.7 ns (277 bits). Error-free operations are achieved under various phase delay
settings (0~+π) between adjacent packets. This implies the circuit is able to apply the right amount of delay to the data based on the mixer outputs, and the DFF always samples in the vicinity of the center of the data eye. The CDR circuit still works if the phase delay is beyond the 0~+π range, but the error analyzer is not able to synchronize with the data because the guard time between the packets changes. The amplitude of electrical input of the BM-CDR circuit is kept above 100 mV, which is specified as the minimum input voltage for the 1:2 fanout according to the HMC720LC3C datasheet. As shown in Fig. 1, an additional BM-LA is required to analyze the BER as a function of input optical power, but it was not available at the time of this experiment. Instead, Fig. 11 shows the measured BER as a function of the optical signal-to-noise ratio (OSNR). The OSNR is measured with a optical spectrum analyzer (OSA) with the resolution bandwidth set to 0.1 nm. In the back-to-back (BtB) measurement, synchronous packets are sent directly to the error analyzer after O/E conversion. The other two BER curves are taken for asynchronous packets with the BM-CDR circuit in front of the error analyzer. The two TDL settings (30 ps and 10 ps) correspond to the best case and the worst case in Fig. 9. The OSNR penalty at 1E-9 BER is 1 dB.

In the experiment, the same clock source is used for the 10-Gbps NRZ-OOK transmitter and the BM-CDR circuit. However, the proposed BM-CDR technique can still work when there is a frequency offset between the extracted clock and the local reference clock. Based on the typical frequency stability of ±5 part-per-million (ppm) of the commercially available electrical 10-GHz local oscillators, the proposed BM-CDR circuit can accommodate packet length up to 25,000 bits without error if allowing a 25-ps deviation from the optimum sampling position for the 10-Gbps data packets. For longer packets, the selection of the data path with optimal phase alignment can be achieved by monitoring the mixer outputs over the entire packet duration and making necessary changes on-the-fly to the 4:1 selector (HMC958LC5). The 4:1 selector supports a maximum select rate of 14 GHz. Error-free operation is verified when reconfiguring the selector during the middle of data packet transmission in the experiment. Since the 4:1 selector only needs to be reconfigured every 5 µs in the worst case scenario, the task can be handled by the FPGA used in the experiment.

IV. CONCLUSION

A 10-Gbps BM-CDR circuit based on analog phase-picking method is presented. The experiment demonstrates that the proposed BM-CDR circuit is able to align the burst-mode incoming data packets to the local clock with a phase alignment accuracy of ±π/4 within 25 ns. Future work will focus on reducing the latency introduced by the circuit and improving phase alignment accuracy.

REFERENCES