2D and 3D heterogeneous photonic integrated circuits
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ABSTRACT

Recent advances in photonic integration demands an addition of a new dimension in integration. 3D integration emerges as a new necessity in providing functional integrated Microsystems for modern computing, networking, and imaging applications.

Keywords: 3D integration, photonic integration, laser inscription

1. INTRODUCTION

Exponential increases in the amount of data that need to be sensed, communicated, and processed are continuing to drive the complexity of our computing, networking, and sensing systems. High degrees of integration is essential in scalable, practical, and cost-effective Microsystems. In electronics, high-density 2D integration has naturally evolved towards 3D integration by stacking of memory and processor chips with through-silicon-vias. In photonics, too, we anticipate high-degrees of 3D integration of photonic components to become a prevailing method in realizing future Microsystems for information and communication technologies. However, compared to electronics, photonic 3D integration face a number of challenges. This paper will review two methods of 3D photonic integration --- fs laser inscription and layer stacking, and discuss applications and future prospects.

2. 3D INSCRIPTION BY FEMTOSECOND LASERS

Direct laser writing of waveguides in dielectric material is an extremely powerful fabrication technique [1]. It utilizes the multi-photon nonlinear absorption of sub-bandgap photons to create permanent structural changes in a material with dimensions comparable to the writing laser’s wavelength (e.g., ~1 µm3). The types of structural changes include refractive index and an increased susceptibility to chemical etching. The induced modifications from a sub-picosecond train of optical pulses are strongly localized in three dimensions to the high intensity region at the focus of a lens driven by a nonlinear absorption mechanism. This unique characteristic is what provides direct laser writing its biggest advantage over other waveguide fabrication techniques; the capability to freely form true three dimensional structures[2]. Direct laser writing has been widely demonstrated in many types of materials including amorphous glasses and crystals with measured losses as low as 0.1 dB/cm (Optoscribe, Ltd specification) [3, 4] in fused silica, and, as an initial demonstration, 0.65 dB/cm [5] in gallium lanthanum sulphide (GLS). This value is expected to go down to 0.1 dB/cm with writing process optimizations (bulk absorption loss for GLS is less than 0.045 dB/cm).

Among many chalcogenide glasses [6], GLS is particularly attractive for infrared applications, since it is transparent from 0.5–10 µm, is commercially available, is arsenic free, is thermally stable up to 550°C, and has a high bulk damage threshold (> 250 MW/cm2 measured) [7]. In fact, unlike many chalcogenide glasses, GLS has been demonstrated for high-power fiber delivery (5W in a single fiber [8]) and as the host material for high-power fiber lasers (10 W pump, 2 W output [9]). Furthermore, recent demonstrations showed that high-quality three-dimensional waveguides are readily created with laser writing speeds on the order of 30 mm/s [10]. Lastly, optical mode sizes can be adapted for a particular application by using waveguide shaping or multiple scan techniques [11, 12]. Figure 1(a) illustrates the direct laser writing process that will be used to write the emitter waveguides into the 3D block. For visible and near infrared applications, fused silica is widely used for 3D waveguide inscription. Figure 1(b) shows a fabricated 3D waveguide fan-out device composed of directly laser writing butt coupled to a 2D waveguide block for orbital angular momentum applications [13-17]. In addition to GLS and silica, zinc selenide (ZnSe) is also a possible candidate 3D block material since it is transparent from 0.5–20 µm and, although not as mature, direct laser writing of low loss waveguides in ZnSe has been demonstrated [18-20].
Similar laser inscribing method can be applied to SU-8 or other UV sensitive polymers for multi-photon induced polymerization of negative-tone resist in the focus of a pulsed laser beam with large numerical aperture. Figure 1(c) illustrates this process where polymerized resist will survive and unexposed resist will be developed away after fs laser exposure followed by developer. Figure 1(d-e) show free-form photonic wire bond created by 3D writing process, and Figure 1(f) shows silicon photonic chip to chip interconnects realized by this photonic wire bonding.

Figure 1. (a) Illustration of 3D waveguide fabrication by direct laser writing using a focused femtosecond laser. (b) Illustration of a 3D waveguide butt coupled to 2D waveguide for orbital angular momentum applications [21] (c) (From [22]) Artist impression of a photonic multi-chip system based on photonic wire bonding. Photonic chips (Chip 1, Chip 2) and optical fibers are mounted on a common submount and embedded into a photosensitive resist. Two-photon polymerization in the focus of a pulsed laser beam is then used to define three-dimensional freeform photonic wire bond (PWB) structures in the volume of the resist. (d) (From [22]) Fabricated photonic wire bonds (PWB) and optical characterization setup. PWB prototype connecting two SOI waveguides on the same chip. The PWB waveguide core consists of SU-8 and features a rectangle-like cross section of approximately 2 μm width and 1.6 μm height. (e) (From [22]) PWB chip-to-chip interconnect: The SOI waveguides are displaced with respect to each other by approximately 25 μm in the horizontal and by approximately 12 μm in the vertical direction. The PWB apex reaches a height of 18 μm above the top surface of the upper chip (Chip 2). Index matching liquid was used to emulate a low-index cladding material, residues of which are still visible on the surface of the chip. (f) (From [22]) Optical characterization setup of a PWB assembly linking two SOI chips (Chip 1, Chip 2). Light is coupled to the SOI waveguides using standard single-mode fibers (‘Input fiber’, ‘Output fiber’) and conventional grating couplers.

Figure 2(a) shows microscope images of single-mode waveguides and their corresponding near-field intensity patterns in GLS at 3.39 μm and at 10.6 μm; demonstrating the capabilities of the 3D buried waveguide technology [10]. Figure 2(b) is an example of a waveguide emitters arranged in 2D for the MWIR and LWIR. Figure 2(c) presents our BPM simulations of the direct laser written waveguides in GLS where the waveguide size has been optimized to produce a minimum mode size for each wavelength of interest; 2.5 μm, 4.6 μm and 9.5 μm (a 2% index contrast in GLS is used), which are the design values of the mode sizes in Figure 2(c).
Figure 2. (a) Microscope images of single-mode waveguides in GLS at 3.39 µm and GCIS at 10.6 µm and their corresponding near-field intensity pattern [10]. (b) Example of a waveguide emitters arranged in 2D for the MWIR and LWIR [10]. (c) Our BPM simulations of the optical modes from directly written square waveguides in GLS at 2.5 µm, 4.6 µm and 9.5 µm (black line designates core region).

Figure 3. Photograph of a direct laser writing arrangement at the author’s laboratory at UC Davis.

Figure 3 shows a photograph of the direct laser writing system at UC Davis capable of precisely writing waveguides in a 150 mm × 150 mm × 25 mm volume with < 0.2 µm accuracy and < 100 nm repeatability. Through these improvements, we propose to develop optimized writing processes for the three spectral bands (SWIR, MWIR, and LWIR) and to explore new techniques such as grading the index in waveguide tapers for reduced coupling losses and enhancing the waveguide index contrast for realizing more compact and lower loss 3D waveguide blocks.

The induced modifications from a sub-picosecond train of optical pulses are strongly localized in three dimensions to the high intensity region at the focus of a lens driven by a nonlinear absorption mechanism. This unique characteristic is what provides direct laser writing its biggest advantage over other waveguide fabrication techniques; the capability to freely form true 3-D structures. We take advantage of the 3-D capability to create the geometric transformation needed to convert linear phase tilt to azimuthal phase variation. Figure 5(a) shows how this concept is implemented using a silica PLC (to convert input position to a linear phase tilt) whose output is coupled to a 3-D PIC for geometric transformation.

Figure 4(a) shows the integratable orbital angular momentum multiplexing device’s operating principle which relies on converting linearly varying spatial phase to azimuthal variations [i.e., $\exp(ib\ell x) \rightarrow \exp(i\ell \phi)$, where $b$ is the linear ($x$) to azimuthal ($\phi$) scaling factor]. To illustrate, Figure 4(a) shows a waveguide circuit where each single mode input (i.e., $\ell = -2, -1, 0, +1, +2$) will create a wavefront in the free-propagation region (FPR) with a different linear tilt. The phase-matched waveguides after the FPR sample the tilted phase front and maintain the phase tilt to the output apertures. Since the apertures are arranged in a circular pattern, they create a beam (coming out of the page) with azimuthally varying phase having topological charge $\ell$. If multiple inputs are illuminated, those inputs are multiplexed onto collinear OAM
beams with $\ell$-numbers determined by the input position. By reciprocity, if an outside OAM beam illuminates the apertures, the sampled light will be focused in the FPR to a waveguide corresponding to the beam’s $\ell$-number (i.e., an OAM demultiplexer). Working as a demux (i.e., OAM state decoder), Figure 4(b) shows how a circular array of waveguide grating couplers are used to sample areas (dashed circles) of an incoming beam encoded with an OAM state (e.g., $\ell = 1$) into a corresponding array of single-mode waveguides. Careful waveguide layout ensures that they have identical optical path lengths. Thus, at the input of the free-propagation region (FPR), the azimuthally varying phase of the OAM state is converted into a linear phase front with a tilt angle determined by the incoming beam’s topological charge, as indicated in Figure 4(a). The circular placement of the array waveguides at the input of the FPR focuses the light, and the tilt of the linear phase front directs it to a corresponding output. Using the PIC as a mux is as simple as reversing the light’s propagation direction. This paper demonstrates a full coherent optical communication link including a pair of silicon photonic OAM mux/demux devices.

![Diagram](image_url)

Figure 4. (a) Visualization of the electric field of OAM beams. (b) Illustration showing how a beam encoded with an OAM state is sampled and demultiplexed by a circular arrangement of apertures, length-matched waveguides and a star coupler.
Using our design \cite{14, 17}, the 3-D PIC was fabricated at a commercial foundry in bulk borosilicate glass and the waveguides had a ~10 µm mode field diameter (i.e., similar to SMF). Figure 5(b) presents a close view of the 3-D PIC output face showing the circular arrangement. Figure 5(c) shows a photo of the fabricated PLC. The waveguides on the silica PLC have a Δn of 2%. Electrical heaters on each output waveguide provide thermo-optic phase-error correction (PEC). This is used to phase match the waveguides between the FPR and the output face of the 3-D PIC. Both the PLC and the input of the 3-D PIC use a 127-µm waveguide pitch. The hybrid device (i.e., PLC and 3-D PIC) is ~30-mm long and the waveguides on the output face form a 204 µm diameter circle with a center-to-center spacing of 40 µm (see Figure 5(d)).
Figure 6(a) shows the silica PLC had an average excess loss of 3.5 dB[14, 17], while the 3-D PIC had an average excess loss of 1.7 dB. To characterize the how well the hybrid device (PLC and 3-D PIC) created OAM modes, we imaged the device’s output (i.e., near-field) onto an IR camera with a total magnification of ~50× while illuminating only one PLC input at a time. The absolute phase (to within a constant) was measured using shearing interferometry. Figure 6(b) shows a false-color (linear scale) image of the near-field intensity and phase patterns when input $\ell = 0$ is illuminated without PEC. Figure 6(c) shows the improvement with PEC (nearly same phase, correct for $\ell = 0$). Figure 6(d) is a plot of the phase for each output waveguide to more clearly show the improvement with PEC. The output phase was then similarly measured for each device input ($\ell = -7, \ldots, 0, \ldots, +7$) and the unwrapped phase is plotted in Figure 6(e). To estimate the OAM mode purity we can take the Fourier transform of the near-field amplitude and phase data for each of the device inputs. Figure 6(f) shows how well the device creates each OAM mode where the difference between a mode peak and the “noise” determines the OAM mode purity or crosstalk (below −12 dB). Figure 6(g-i) show the measured near-field pattern intensity and phase for several different example OAM modes (typical).

3. 3D STACKED PHOTONIC INTEGRATION

Figure 7. Future 3D processor consisting of silicon photonic interconnect plane, memory plane, and processor plane together with an external optical frequency comb source.

Silicon photonics exploits the CMOS infrastructure built up on many billions of dollars of investments in the past. While the photonic devices are quite large in physical size and fabrication resolution compared to the electronic devices, thus the number of devices to be integrated in the die can be orders of magnitude lower, the uniform and well-established CMOS fabrication platform can contribute greatly to manufacturability of photonic components for future computing. Initially, silicon photonics stirred speculations that the future CMOS will combine photonic integration and electronic integration, which expect to bring significant impact by (a) offering intelligent data processing and storage capabilities of electronics together with high capacity and parallelism of photonics, or by (b) realizing signal processing in the photonic domain. However, challenges of photonic-electronic integration lie in the process compatibility between photonic and electronic ICs, isolation, crosstalk, yield, and heat density. The groups at Luxtera, IBM, and MIT/Micron have recently and independently demonstrated electronic-photonic integration on a silicon CMOS platform [23]. More practical photonic-electronic integration would be to pursue hybrid integration by die bonding or wafer bonding. As Figure 7 illustrates, 3D photonic-electronic integration can build up on the already active 3D electronic integration with through-silicon-vias (TSVs) together with photonic integrated circuits.

In the following, we discuss 2D silicon photonic integrated circuits that will be stacked together to form a 3D photonic integrated circuits.
Figure 8 (a) shows the 2D silicon photonic integrated circuit layout which is designed for a silicon-on-insulator (SOI) material platform, optimized for TE polarization, and uses a 1 µm wide silicon rib waveguides (effective index of 3.27). The upper inset of Figure 8(a) shows a quarter of the circular grating which is formed by concentric etched circles that have a grating period of 0.47 µm, a 50% duty cycle, and an outer radius of 25 µm. The circular grating converts the vertically incident optical beam (azimuthal polarization) into a horizontally propagating beam. Sixteen tapered waveguides surround and capture the light from the grating and send it to length-matched waveguides (20 mm long) that terminate at the FPR [lower inset of Figure 8(a)]. Depending on the OAM state of the input beam, the 16 guided modes will have a specific linear phase variation. Since the FPR is designed based on the Rowland circle principle, it focuses the 16 beams onto five waveguide outputs according to the linearly varying phase associated with the five different OAM states (labeled as ℓ = +2, +1, 0, −1, −2). The five waveguide outputs are tapered to a 3 µm width at the edge of the chip and have 250 µm spacing. The device also includes aluminum contact pads and traces that connect to sixteen Ti/Pt heaters. The heaters, located just above the waveguides, thermo-optically change the local index of refraction to compensate for optical phase errors (<π rad) in the waveguides.

Figure 8 (b) shows the OAM device fabricated on a 6 inch silicon-on-insulator (SOI) wafer with a top silicon layer thickness of 0.5 µm, and buried oxide (BOX) layer thickness of 3 µm. The waveguide layer was patterned using deep-UV ASML stepper with 248 nm KrF excimer source and 4:1 reduction, then transferred to the silicon layer by a 250 nm deep highly anisotropic HBr TCP reactive ion etch. The subsequent stepper lithography and etching process was similar to the previous steps and defined the circular grating layer with an etching depth of 200 nm. The inset of Figure 8(b) shows a scanning electron microscope (SEM) image of the fabricated grating. Next, the wafer was clad with 1 µm thick SiO2 by low pressure chemical vapor deposition (LPCVD) and then annealed for densification at 900°C for 40 minutes in an inert atmosphere. The LPCVD SiO2 coating isolates the waveguide mode from the surface metal layer, eliminating the loss due to metal absorption. Ti/Pt heaters were deposited with an e-beam evaporator and defined through liftoff. The heaters provide phase control on the length-matched waveguides. As a final step, aluminum electrodes were deposited and defined with another liftoff process.

We have extended a similar fabrication technique to silicon nitride/silicon oxide waveguide system and utilized multi-layer stacking of OAM device layers. Figure 9 shows stacking of multiple 2D layers for arbitrary waveform shaping, (a) stacked device consisting of Layer 1-5, and (b) fabricated three layer silicon nitride/silicon dioxide OAM device. Also shown are the images of the three layer silicon nitride/silicon dioxide OAM device when the (c) bottom (layer 1), (d) middle (layer 2), and (e) top (layer 3) are illuminated. When multiple layers are coherently excited, this device can create mode profile that can excite eigen modes of the multimode fibers.
4. CONCLUSION

3D photonic integration emerges as a powerful new dimension to the current photonic integration platform. Laser inscribing provides a free-form method to create arbitrary shape embedded waveguides in 3D and also offers a method to achieve photonic wirebonding. Multilayer stacking facilitates creation of 3D photonic integrated circuits by using conventional lithography and deposition methods. 2D/3D heterogeneous photonic integration is essential for future computing, networking, and imaging systems aiming at scalability, high-performance, and cost effectiveness.

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REFERENCES


