High-Density Wafer-Scale 3D silicon-photonic integrated circuits

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Abstract—This paper discusses recent advances on the newly-developed high-density 3D photonic integrated circuits (3D PICs). In particular, we introduce our efforts in design, fabrication and characterization towards a silicon photonic wafer-scale light detection and ranging (LIDAR) system populated by 3D PIC unit cells. The 3D PIC unit cell includes vertical U-shaped photonic couplers created by a combination of anisotropic etching, vertical α-silicon via formation and wafer-bonding. Using the U-shaped photonic couplers, the 3D PIC unit cell forms a 120-channel folded single tile optical phased array (OPA) with 2μm pitch. Ultra-compact vertical U-shaped coupler arrays with 1μm pitch are also fabricated and tested. The 3D PIC unit cells will be tiled on a wafer-scale interposer, transmitting and receiving signals through equal-power splitters with pathlength-matched waveguides, and 3D arbitrarily-shaped waveguides or evanescent couplers. Designs of such interposers are shown and low-loss and misalignment tolerant chip-to-interposer coupling using evanescent coupler is demonstrated. Loss values of arbitrarily shaped waveguides fabricated by ultrafast laser inscription (ULI) on the deposited-SiO₂ cladding and their alignment tolerance to conventional silicon nitride (SiN) edge couplers are reported. A path towards realizing 3D integrated LIDAR are discussed.

Index Terms—Silicon photonics, Photonic integrated circuit, Three-dimensional integrated circuits, Nanofabrication, Phased arrays, Laser radar.

I. INTRODUCTION

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corollary, the Dennard’s law [6] claimed that the power-efficiency will also scale at the same pace with the Moore’s law. While this remarkable exponential scalability in integration still continues today after five decades, the Dennard’s law stopped keeping pace with the Moore’s law in 2004 because of the skin effects and impedances of electronic interconnects. Hence, high-density integration has extended to 3D integration by stacking multiple layers of 2D EICs using through-silicon-vias (TSVs) [7]. 3D EICs offered a number of performance enhancements over 2D EICs [8]: (a) lower power consumption due to reduced number of repeaters and equalizers on shorter communication distances, (b) lower noise and jitter on shorter interconnects, and (c) higher packing density in 3D. On the other hand, photonic integration efforts so far mostly stayed with 2D (2D PIC) because it already offered high channel capacity and high bandwidth thanks to wavelength division multiplexing (WDM) while avoiding similar constraints due to skin effects and impedance. 3D photonic integration has recently emerged as very important steps for bringing new functionalities and high degrees of integration to microsystems [9-18]. 3D Photonic Integrated Circuits (3D PICs) overcome many limitations of 2D PICs where all photonic components must reside on the same plane. As we will discuss in the following sections, 3D PICs allow multiple functionalities on multiple planes of 2D PICs to achieve combined functions on a limited footprint. 3D PIC based on silicon photonics is extremely important because it combines low-energy operation, high-density functionalities, and high-yield manufacturing on a CMOS platform already developed for 3D electronic integration. This paper discusses design, fabrication, and characterization results of new high-density 3D photonic integrated circuit being developed for LIDAR imaging systems.

II. HIGH-DENSITY WAFER-SCALE OPTICAL SYSTEM: AN SCALABLE LIDAR SYSTEM AS AN EXAMPLE

We consider a wafer-scale LIDAR system schematically illustrated in Fig. 1. It consists of 3D photonic integrated circuit unit cell tiled on a wafer-scale interposer. The wafer-scale interposer acts as an optical backplane with electrical connections for the tiling of the unit cells. Each unit cell (1 cm
A coherent light signal will propagate through the interposer and distributed to each unit cell through the interposer, and the reflection signals will be collected by each cell and will be relayed to the photodetectors on the interposer. On each unit cell there will be two photonic layers, namely top emitting aperture (e.g., grating arrays) and active photonic layer containing splitters and phase modulators, vertically integrated with control ASIC unit that lies in between the unit cell and the interposer. In order to achieve large lateral beam steering angles, each emitting element ideally need to be packed with half wavelength pitch [19]. Depending on the application requirements, unit cells can be tiled to 10 × 10 arrays with the emitting aperture area that cover > 95% of the total footprint.

Sec. III details the design and fabrication of the vertical U-shaped couplers and a proof-of-concept illustration of silicon photonic unit cell OPA. Sec. IV presents our design and current characterization of a wafer-scale interposer and its coupling to silicon photonic unit cell. Sec. V introduces our latest result of vertical arbitrarily curved waveguides inscribed in deposited oxide cladding.

III. ULTRA-COMPACT SILICON PHOTONIC VERTICAL U-SHAPED COUPLER

Here, we discuss the design and fabrication of the vertical U-shaped coupler as a key enabling technique for high-density 3D PIC. We have proposed and demonstrated vertical U-turn shaped coupler using standard CMOS compatible fabrication technologies. Unlike the previous demonstrated optical TSVs [20] with ~100 μm diameters, these couplers and vias can be fabricated with standard silicon waveguide dimensions without the time consuming deep etching or angled dicing [21]. As all components can be aligned and fabricated using a projection lithography tool (stepper), the alignment error can be controlled to within a few tens of nm, no additional packaging is required [22]. Owing to the strong confinement of the silicon waveguide, it can be packed with a subwavelength pitch in contrast to the conventional inverse-taper based evanescent couplers.

A. Concept, Design and Simulation

Fig. 3 (a) reveals the detailed structure of the vertical U-shaped coupler. It consists of two 45° reflectors connecting to different silicon waveguiding layers and an interlayer vertical optical via. The silicon layer thickness is set to be 500 nm to facilitate light coupling to other materials like InP for efficient electro-optical modulation [23]. The transition to 220 nm-thick silicon waveguides can be made through lateral/vertical tapers with negligible loss [24]. All waveguides are fully etched to form wire-waveguides to reduce coupling to the adjacent elements. Fig. 4 (b) shows a simulated light transmission from the bottom silicon layer to the top layer using a finite-difference time-domain (FDTD) tool. With proper design of the U-shaped coupler parameter, it is possible to achieve 74% light transmission within a 1 μm³ volume.
Fig. 3. (a) Perspective schematic of the ultra-compact vertical U-shaped coupler consisting of a silicon photonic vertical via and two 45° reflectors. (b) FDTD simulated transmission of the vertical U-shaped coupler from the bottom layer to the top layer.

We studied the parameter dependent light transmission properties of the U-shaped coupler using the FDTD tool shown above. We defined the offset as the center-to-center shift between the 45° reflector and vertical via, \( d \) as the vertical via length along the silicon waveguide directions, gap as the distance between the top and bottom silicon layers. Figs. 4 (a) –(c) show our calculated the interlayer light intensity transmission upon different parameters defined above. We fix the waveguide width in the vertical U-shaped coupler region to be 800 nm to increase both the light transmission and fabrication tolerance. In calculation shown in Fig. 4(a), we set \( d = 500 \text{ nm} \) and \( \text{gap} = 1000 \text{ nm} \) and observed only fundamental mode is excited for offset larger than 75 nm. The maximum transmission of 0.66 is obtained when the offset is 125 nm. We then fixed the offset to be 125 nm and the gap to be 1000 nm to optimize the \( d \) of the vertical via. We obtained a maximum transmission of 0.71 when \( d = 450 \text{ nm} \). Finally, we optimized the gap between the two silicon layer and achieved a maximum transmission of 0.74 with \( \text{gap} = 1300 \text{ nm} \). Current waveguide design support multimode and we are designing 300nm Si based vertical U-shaped coupler to eliminate the higher order mode excitation in the top silicon emitting layer.

Fig. 4. Simulated transmission of the vertical U-shaped coupler as a function of (a) center-to-center offset, (b) via length and (c) interlayer gap using FDTD method.

B. Device Fabrication

Fig. 5 illustrates the detailed fabrication process of the vertical U-shaped coupler connecting two silicon photonic layers.
We started our fabrication of the 3D integrated silicon photonic PIC on a 6-inch silicon-on-insulator (SOI) wafer with 500 nm thick silicon device layer. The first 45° reflector (Fig. 6(a)) was etched using a TMAH-based solution and etching naturally stopped at the buried oxide (BOX) layer [25]. Fig. 6(b) shows the tiled view of scanning microscope image (SEM) of an etched mirror on a dummy silicon wafer, revealing a smooth reflecting surface. We expect the surface roughness value on the etched mirror is less than 10 nm [26].

Then we patterned splitters and waveguide arrays in the same silicon layer and deposited 2.5 µm oxide cladding. After planarization using chemical mechanical polishing (CMP), we transferred the fabricated waveguide arrays with the reflectors on a thermal oxide on silicon wafer.

We then patterned silicon photonic vertical optical vias with deep oxide etching, α-Si filling and excess α-Si polishing [27]. Fig. 6(c) shows the cross-sectional SEM of fabricated vertical optical via on an oxide dummy wafer. We achieved a high aspect ratio (~2.5:1) via with subwavelength pitch (Fig. 6(d)) by carefully optimizing lithography and etching conditions. We measured the material loss of the deposited α-Si film using an ellipsometer. Measured k value is <0.017 in 1500 – 1600 nm range, corresponds to an absorption loss < 0.6 dB in 1 µm length. This loss can be further reduced using hydrogen annealing.

We transferred a 2nd single crystalline silicon layer using oxide direct bonding. Using the same wet etching recipe, we formed the upper 45° reflector and completed vertical U-shaped coupler. Fig. 6(e) and (f) show the cross-sectional and perspective view of fabricated vertical U-shaped structures after partly removed oxide cladding.

C. Preliminary Characterization and Proof-of-Concept Demonstration of Optical Phased Array Unit Cell

We measured vertical U-shaped coupler transmission loss using a cascaded interlayer coupling test structure (Fig. 7 inset). Fig. 7 shows our measured loss upon different offset design and we extracted a minimum loss of 8.4 dB per coupler at offset = 130 nm (bottom) and 425 nm (top). The relatively high measured loss is mostly due to a large misalignment between the top 45° reflectors and the vertical vias (~300 nm larger than the designed value), and due to the excessive etching that
caused $\alpha$-Si scattering near the reflector (both can be seen in Fig. 6 (e) and (f)). These fabrication errors contributed to 4-5 dB additional loss as suggested by our FDTD simulation. We are now improving our alignment accuracy using a Vernier ruler based structure for misalignment correction and further controlling the $45^\circ$ etching undercut using a test structure. Expected misalignment can be reduced to below 50 nm as suggested by the value between bottom silicon layer and vertical via. Other design and process optimization are also on-going to reduce the $\alpha$-Si absorption loss and higher order mode induced loss. These will help achieve low loss coupling at ~1.3 dB as simulated.

Fig. 7. Measured transmission loss of cascaded vertical U-shaped coupler test structure.

Fig. 8 (a) shows the optical microscope image of a fabricated 120-channel 2$\mu$m pitch OPA device using the similar fabrication process shown in Fig. 5. It has a $1 \times 128$ MMI tree based splitter (Fig. 8 (b)) and with silicon thermal-optical phase modulators (Fig. 8 (c)) on the top silicon layers. Each waveguide then fans in into 2$\mu$m pitch and transport light into the bottom grating emitter array through the vertical U-shaped coupler (Fig. 8 (d)). The emitting aperture area is 0.25 mm $\times$ 5 mm and its fill-factor is currently limited by the thermal crosstalk between the thermo-optic phase modulators, and the InP/Si based dense phase modulator array is currently under development to realize large fill factor (~95%). We measured a grating emitting strength of ~23 dB/cm for our partially etched SiN assisted grating, which radiates more than 90% of the total power during 5 mm propagation. The grating section can be further optimized using a chirped design for uniform power emission for tiles integration.[28] Fig. 8 (e) – (g) show the detailed fabricated structures the partially etched SiN assisted grating. The preliminary experiment indicated successful light transmission through the 3D integrated silicon photonic unit cell with approximately 8 dB loss. The full characterization of this 3D integrated silicon photonic unit cell is currently in progress and will be a subject of a future publication.

Fig. 8. (a) Optical microscope image of fabricated proof-of-concept 3D integrated silicon photonic unit cell. Zoom-in of (b) the MMI tree based splitter, (c) the heater based thermal tuners, (d) the two silicon photonic layers with U-shaped couplers and (e) the 2$\mu$m pitch waveguide grating array. (f) Top view and (g) cross-sectional view SEM pictures of fabricated partially etched SiN assisted grating.

IV. WAFER-SCALE INTERPOSER: OPTICAL BACKPLANE

We designed a wafer scale optical interposer (WSOI) based on low-loss compact silicon nitride platform as an optical backplane for the wafer-scale PIC. Fig. 9 shows our calculated design trade-off of the SiN core thickness. In order to balance the waveguide propagation loss, bending radius, chip-to-interposer coupling loss, and fabrication tolerance (See Sec. IV B), we choose the SiN core thickness to be 100 nm, waveguide width to be 3 $\mu$m and bending radius to be 500 $\mu$m. Based on our previous fabrication runs, expected waveguide propagation loss is < 0.1 dB/cm.

A. Wafer-Scale Equal Power Splitting and Pathlength-Matched Design

The WSOI needs to deliver the power to each silicon photonic unit cell based tile with uniform power and phase to ensure the large coherent aperture operation and mitigate the system sensitivity to pathlength dependent loss and phase errors. Fig. 10 shows the layout of the WSOI with equal power splitting and a pathlength matched design to $10 \times 10$ tiles. Power from the external laser will be evenly distributed to each tile through cascaded $1 \times 10$ star couplers and then evanescent coupled to the silicon photonic unit cell above. The total waveguide length to each tile from the laser input is fixed at 15 cm, which gives less than 1.5 dB loss with the SiN core thickness of 100 nm.
Fig. 9. (a) SiN core thickness and corresponding minimum waveguide width. (b) The relationship between confinement factor and minimum bending radius with waveguide core thickness.

The projection lithography gives higher resolution with lower side wall roughness compared to the contact lithography, but the exposed field is typically limited to ~22 mm × 22 mm. On the other hand, the contact lithography can expose the full 150 mm wafer but at much-reduced resolution. To fabricate the WSOI with fine features for the power splitter and evanescent couplers, we combine the contact lithography and the projection lithography. Waveguide connections (3 μm wide) on the WSOI will be first exposed using the contact lithography and then splitters and evanescent couplers butt connected to the waveguide will be exposed using a stepper with proper stitching methods. By using appropriate alignment marks and correction methods, it is possible to control the misalignment at the waveguide junction to be less than 100 nm. We simulated the stitching induced loss using our FDTD tool and expected the loss to be within 0.01 dB per junction when misalignment is 100 nm (Fig. 12).

Fig. 10. Path length matching and stitching design of WSOI.

Fig. 11 (a) shows our equal power splitting funnel type star coupler design. The output aperture width is tapered from center to edge to ensure the same amount of power being captured from the Gaussian profile in the free propagation region. Our calculated result suggests a ~ 1 dB from the splitter with power variation between the ports to be less than 0.1 dB.

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Fig. 11. (a) Layout of the equal power splitter. The output width and power are shown in (b) and (c) respectively.

Fig. 12. Diagram of waveguide stitching and modal and results of FDTD simulation on waveguide stitching. The arrow denotes the incident direction.

B. Optical Coupling from Interposer to Silicon Photonic Unit Cell

Before the ASIC and 3D ULI integration, we packaged our silicon photonic unit cell to WSOI using SiN evanescent couplers (vertical gap ~1 μm compared to 40 - 80 μm with ASIC). The vertical light coupler from the WSOI to silicon photonic chip consists of two inverse tapers on the WSOI and the silicon photonic chip, respectively [29]. We design the overlapping length of the inverse tapers to be 500 μm and the
The final taper width to be 250 nm (limited by the stepper). The overcladding oxide thickness on top of SiN inverse taper is set to 400 nm to facilitate light coupling from WSOI to silicon photonic chip. Fig. 13 (c) shows our simulated transmission with different SiN inverse taper designs. Both designs have negligible coupling loss assuming no misalignment during the packaging. Using 200 nm SiN at the silicon photonic chip will tolerate $\pm 2 \mu m$ misalignment while using 100 nm SiN at both sides will further relax the requirement to $\pm 3 \mu m$. We choose the SiN inverse taper thickness on the silicon photonic chip to be 200 nm to maintain low transition loss from the silicon waveguide. We measured a transition loss of 0.34 dB from 250 nm thick SOI waveguide (Fig. 13 (d)).

For a proof-of-concept demonstration, we perform an Au-to-Au flip-chip bonding for the silicon photonic chip to interposer packaging. We etched a trench on the inverse taper region of the optical interposer and deposited 200 nm Au for alignment (Fig. 14(a) inset) and flip-chip bonding. A counter trench is etched on the silicon photonic chips, so the two inverse tapers will be bonded closely, achieving a low loss inverse taper coupling. During packaging, chips are flip-chip mounted to the interposer by thermal compressive flip chip bonding as shown in Fig. 14 (a). We measured the transmission loss from waveguides transmitting power from interposer to silicon photonic chip and back to interposer. Fig. 14 (b) shows measured coupling loss of the evanescent coupler upon different misalignment. We observed a minimum 3.1 dB loss from the coupler with $1 \text{ dB}$ tolerance to be $\pm 3 \mu m$. We attribute the loss variation within the tolerance band to the unwanted dust in the coupler region.

V. ARBITRARY VERTICAL WAVEGUIDE FOR LOW-LOSS SILICON PHOTONIC UNIT CELL TO INTERPOSER PACKAGING

ULI has become an emerging technology for 3D photonic device fabrication, facilitating 3D photonic packaging [30]. Low-loss 2D-3D fan out chips [31] and photonic wire-bonding [32] have been demonstrated using this technique. However, demonstrated waveguide devices are typically on glass or polymer platforms [31, 32], which generally are not compatible with the mature CMOS fabrication. This prohibits its further application in the photonics/photonics-electronics convergence systems.

Here we proposed a new chip-to-chip optical coupling scheme using an arbitrary vertical S-bend low-loss waveguide fabricated on deposited oxide cladding for 3D photonic packaging. We demonstrated a low propagation loss of 0.8 dB/cm and a less than 3 dB/facet coupling loss to a conventional SiN inverse taper with an alignment tolerance larger than 1 $\mu m$ in both horizontal and vertical directions on the fabricated device. Initial demonstrations are limited to separate chip-to-chip coupling, intra-chip coupling to SiN inverse taper and chip-to-interposer coupling are under development.

A. Waveguide Formation using Ultrafast Laser Inscription

We fabricated a proof-of-concept ULI devices on a 6-inch silicon wafer with deposited oxide cladding using standard low-pressure chemical vapor deposition (LPCVD). The measured wafer bow is less than 30 $\mu m$ upon 40 $\mu m$ thick oxide deposition.
We fabricated 3D ULI waveguides using a femtosecond laser at 1038 nm wavelength. The laser was operated at the rate of 500 kHz with the pulse width of 300 fs and the pulse energy was set to 130 mW. The microscope objective with 0.55 NA was used to focus the beam onto the sample on a computer controlled 3-axis stage as shown in Fig. 15(a). In order to optimize the transmission efficiency of the waveguides, we use a multi-scan technique with a 200 nm lateral shift between each scan and all waveguides were fabricated at a depth of 15 μm with the writing speed of 3 mm/s. Fig. 15(a) inset shows the ULI waveguides on a 5cm long deposited oxide substrate. Fig. 15(b) shows the cross-section picture of a fabricated straight waveguide on deposited oxide sample and Fig. 15(c) shows the corresponding measured single mode profile at 1550 nm. Fabricated waveguide dimensions and measured lateral mode diameter on deposited oxide cladding are comparable to those fabricated on the glass substrate (see Fig. 15(d) and (e)). The ULI waveguide fabricated on the oxide substrate has larger mode diameter in the vertical direction due to the strong reflection from the silicon substrate during the writing.

**B. Loss Characterization**

We fabricated straight and an S-shaped structure with the bending radius of 20 mm and the bending angle of 1 degree on both the deposited oxide substrate and the glass substrate to extract the ULI waveguide loss. We extracted a low propagation loss of 0.7-0.8 dB/cm on both materials. The calculated excess bending loss on deposited oxide sample is relatively high, about 1.4-2.2 dB. We attribute this to the non-optimal writing recipe close to the wafer surface and expect this can be brought down to 0.3-0.4 dB (values on glass substrate is written at 150 μm below the surface).

We simulated the coupling loss from a ULI WG to a conventional SiN inverse taper coupler using a finite-difference mode (FDM) solver. From the measured mode profile, we assume a 0.8% refractive index change in the ULI waveguide core region compared to the cladding region. Fig. 16(a) shows the coupling scheme in the simulation. The SiN waveguide is 200nm thick and adiabatically tapered into the ULI WG core region. Fig. 16(b) summarized the proposed coupling scheme and simulated coupling loss to a conventional SiN inverse taper coupler. We expect the coupling to be less than 1 dB and with sufficiently long taper region, this can be further reduced to be less than 0.5 dB.

We conducted coupling loss measurement between the SiN coupler to the ULI waveguide using two separate chips, as
shown in Fig. 17(a). A vacuum compatible stage was used to stabilize the 3D ULI chip on the stage and a polarization controller was connected to the input fiber to optimize the polarization of the propagation light. Fig. 17(b) shows the fabricated SiN inverse taper using 248nm projection lithography. Given the taper size and measured mode profile (Fig. 17(c)), we expect a ~0.6 dB coupling to fabricate the ULI waveguide.

We measured a minimum coupling loss of 2.8 dB and we attributed the ~2dB excess loss to the air gap between the two chips. We assessed the structural tolerance by measuring the coupling loss as a function of offset from the lowest loss point along horizontal and vertical direction respectively and results are summarized in Fig. 17(d). We observe the negligible loss increment within the 1μm misalignment and less than 2 dB increment within the 2 μm misalignment.

VI. SUMMARY

In this paper, we discussed and demonstrated our design, fabrication and characterization of the key building blocks of a newly-developed high-density 3D PIC that can be used to build a wafer-scale LIDAR system. We demonstrated an ultra-compact vertical U-shaped silicon photonic coupler with ~0.8 μm × 0.5 μm × 1.3 μm size and 1 μm pitch. Simulated transmission loss can be down to 1.3 dB. We fabricated a 120 channel 3D OPA that can be populated on an interposer as a unit cell. We designed the wafer-scale optical interposer as an optical backplane with equally power distribution with matched waveguide length to 10 × 10 unit cell arrays. We fabricated vertical arbitrary shaped ULI waveguide on deposited-SiO₂ cladding with 0.8 dB/cm loss and measured a ±2 μm alignment tolerance when coupled to a SiN edge coupler. These techniques will bring on low power consumption and high-performance 3D PICs such as large aperture LIDAR systems.

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