

# Future prospects of silicon photonics in next generation communication and computing systems

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The recent progress is reviewed and future prospects of silicon photonics in next generation communication and computing systems are probed. Leveraging the many-billion-dollar complementary metal-oxide-semiconductor (CMOS) industry, silicon photonics has promising prospects for realising very large-scale electronic and photonic integrated circuits with thousands of optical components and millions of transistors in the future to support very demanding integrated systems needs of next generation computing and communications. There are also a number of significant challenges in fulfilling such prospects.

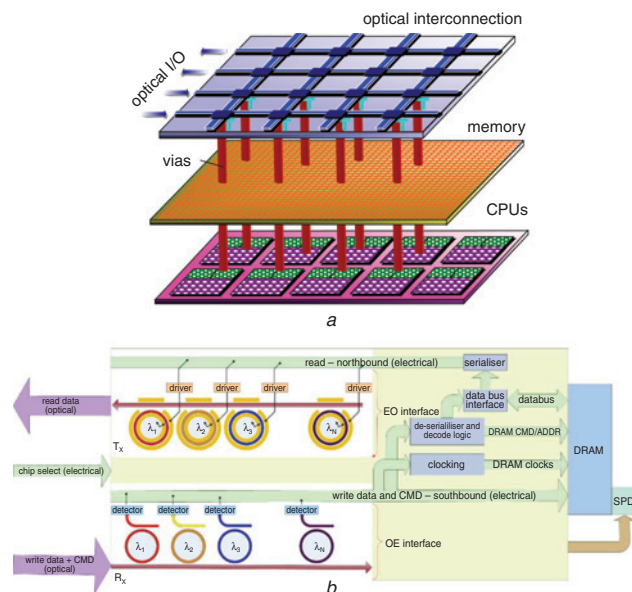
**Introduction:** The capability to cost-effectively integrate photonic circuits and electronic circuits on a single and scalable platform can bring fundamentally significant impacts to many applications including computing, communications and signal processing. Such a capability can combine the benefit of high-capacity and parallelism from photonics together with versatility and intelligence from electronics. There has been a long history of III–V optoelectronic integrated circuits (OEICs) [1, 2] where optical detectors, modulators, multiplexers/demultiplexers, or lasers are integrated with electrical amplifiers or other electronics on the same platform. From the beginning, OEIC technology development was considered to be a high-risk and high-reward undertaking. Photonic integration alone (without electronics) can potentially bring significant reduction in cost, power consumption, size and even failures from (a) reduction in the number of discrete components, (b) reduced packaging requirements (including thermoelectrical coolers), and (c) fewer optical coupling interfaces. However, the challenges have been the practical and sustainable yield, the material and processing compatibility, and the signal and thermal crosstalk isolation. The benefits of electronic–photonic integration can be potentially even greater than those of photonic integration; however, the challenges from the yield and material/fabrication compatibility can be insurmountable.

Even today, there has not yet been a large-scale (> 1000 components) OEIC commercially deployed, but rather hybrid integration became more popular, primarily owing to the high development cost, low yield and poor flexibility associated with monolithically integrated fabrication processes. In particular, epitaxial growth and regrowth based integration on relatively small (50–100 mm diameter) InP or GaAs wafers made it difficult to support very large-scale integration (> 10 000 components).

Silicon on the other hand is an excellent optical and electrical material that comes in large wafer sizes backed by billions of dollars in CMOS industry. Silicon exhibits very low optical losses (material losses < 0.01 dB/cm losses in unintentionally doped Si material) at the standard fibre optical communication wavelengths (1.3–1.6 μm). Pioneering works by Soref and Petermann in the late 1980s and early 1990s [3, 4] stimulated substantial activity in silicon photonics. Subsequent introduction of commercial and practical high-volume manufacturing of CMOS electronics on silicon-on-insulator (SOI) wafers significantly accelerated research and development activity in silicon photonics [5]. When standard CMOS foundry processes can be used to fabricate electronic and photonic integrated circuits (EPIC) together, very large-scale EPICs can be envisioned for future integrated systems. Naturally, they combine the versatility and intelligence of electronics and the benefit of high-capacity and parallelism of photonics. This powerful combination fundamentally impacts a wide range of applications, including computing, communications and signal processing.

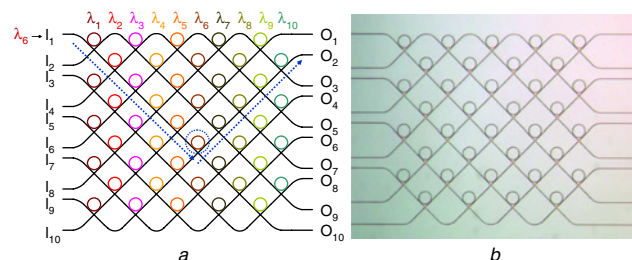
**Silicon photonics in computing [6, 7]:** In 2007, the Intel research team announced an 80-core Polaris chip with 1 teraflops. It is expected that computer chips in 2020 may contain 1000 cores with ultra-high-density nanoscale devices exceeding 10 teraflops in performance. This trend casts new challenges in communication and power requirements. Amdahl's law [8] suggests that a system with balanced computation and communications performs the best under most circumstances. A 10 teraflops chip would require an interconnect bandwidth of 100 Tbit/s for a balanced architecture. This is 20 times greater than

the average 5 Tbit/s Internet traffic in the USA today! Further implications of Amdahl's law are that the 10 teraflops system will need a 10 Tbyte of RAM with 100 Tbit/s I/O bandwidth. These growing imbalances and constraints have driven computer architectures in the past several decades to evolve by seeking performance compromising solutions, for instance, by emphasising the locality and hierarchy of data access with limited bandwidths.



**Fig. 1** Optically interconnected future multicore processors with three planes: CPU, memory and optical planes interconnected by vias; and optically connected dual inline memory module (OC-DIMM) with optical memory controller (OMC) [18]

a Future multicore processors  
b Dual inline memory module



**Fig. 2** Optical interconnection crossbar architecture and fabricated chip where micro-resonators provide wavelength dependent routing and interconnection

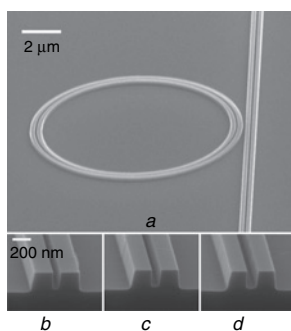
a Architecture  
b Fabricated chip

Silicon photonic interconnects offer a disruptive technology solution that fundamentally changes the computing architectural design considerations. Optics provide ultra-high throughput, minimal access latencies, and low power dissipation that remains independent of capacity and distance. For a distance exceeding a few millimetres, the energy efficiency of electrical signalling is typically ~10 pJ/bit (equivalent to ~10 mW/Gbit/s), and future generations may reduce this to ~2 pJ/bit [9]. With 10 pJ/bit, 1000 W is required just to support the interconnect bandwidth at 100 Tbit/s. Optical communication links based on nanoscale silicon photonics have shown the ability to operate at 100 fJ/bit, with future modifications for bringing it down to 10 fJ/bit [10, 11]. In addition to the energy efficiency, many of the fundamental physical problems of interconnects are directly addressed within the optical technology platform, including precise clock distribution [12], bit rate transparency and power reduction, without concerns for impedance [13], crosstalk, voltage isolation, pin inductance, signal distortion and repeater-induced latency. Increasing the DRAM bandwidth by a factor of ~100 on each pin can potentially revolutionise future computing systems. Multi-wavelength photonic interconnects in the DRAM I/O can be envisioned to achieve this performance in a scalable fashion.

The opportunity for optical interconnects [14, 15] in board-to-board and rack-to-rack communications is already well documented. Exciting opportunities exist in wavelength routing to reconfigure the high-capacity connectivity of multiple wavelengths to reduce contention and increase system-wide throughput [16, 17]. Recent advances in silicon nanophotonic technologies compatible with nanoelectronics offer new possibilities in realising future computing systems with a fundamentally new architecture.

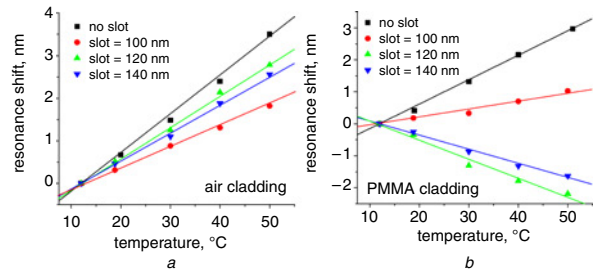
CMOS-compatible silicon photonics offer a practical platform for routing and transporting multi-wavelength optical signals interconnecting electronic processors and memories using the same CMOS fabrication processes that are used in the foundries today. Potentially, a combination of high-yield, high-uniformity and high-volume productivity of CMOS processes can be applied to silicon photonics to realise low-cost and high-quality optical interconnection of computing processors and memories. Fig. 1a shows an example of such a system in three layers: optical interconnection, memory and processor planes, all fabricated by CMOS compatible processes. Potentially, such a system can grow to a  $\sim 1000$  core system optically interconnected by 100–1000 wavelengths where a flattened hierarchy architecture becomes possible. Fig. 1b shows a schematic of an optically connected dual inline memory module (OC-DIMM) with optical memory controller (OMC) employing DWDM optical buses [18]. Fig. 2 shows the optical interconnection crossbar (Fig. 2a) architecture and (Fig. 2b) fabricated chip where silicon photonic micro-resonators provide wavelength dependent routing and interconnection [19].

Practical silicon photonics should also consider athermal operation to account for temperature variations from core-to-core by  $> 15^\circ\text{C}$ . Owing to the high thermal sensitivity of silicon ( $92\text{ pm}/^\circ\text{C}$ ), realistic implementation of dense wavelength division multiplexing (DWDM) on silicon photonics on chip multiprocessors has been difficult (50 GHz DWDM channel spacing would require better than  $0.5^\circ\text{C}$  temperature control). The thermally compensated slotted waveguide design [13] achieves temperature independent operation across a  $100^\circ\text{C}$  temperature range when material with a negative thermo-optic coefficient such as polymethyl methacrylate (PMMA) is filled inside the slot [19–21] so that the resonances can be maintained steady under temperature variations [22–24]. Another advantage of using PMMA cladding is that the resonant wavelengths can be trimmed by UV illumination on the PMMA layer, so that accurate wavelength registration of the athermal silicon microring resonator becomes possible [19]. Fig. 3 shows the scanning electron microscope (SEM) image of the fabricated slotted microring resonators with three different slot widths of 100, 120 and 140 nm. Figs. 4a and 4b show the resonance shift as a function of substrate temperature with air cladding and PMMA cladding [19]. For the air-cladding, the regular microring resonator has the highest thermal sensitivity of  $92\text{ pm}/^\circ\text{C}$ , and the slotted microring with 100 nm slot has the lowest thermal sensitivity of  $48\text{ pm}/^\circ\text{C}$ . For the PMMA cladding, the slotted microring resonator with 100 nm slot also has the lowest thermal sensitivity of  $27\text{ pm}/^\circ\text{C}$ . Both the slotted microring resonators with 120 and 140 nm have negative TO coefficients, which indicates that their thermal coefficients for the waveguides are over-compensated by PMMA upper cladding in both cases [19].



**Fig. 3** Scanning electron micrograph (SEM) image of slotted microring resonator (microring resonator radius  $5\ \mu\text{m}$ ) and zoom-in SEM images of slotted waveguide cross-section with various slot widths

a SEM image  
b–d Zoom-in SEM images with slot widths of b 100 nm,  
c 120 nm and d 140 nm  
Waveguide width fixed at  $0.5\ \mu\text{m}$  [19]



**Fig. 4** Resonance shift against substrate temperature for slotted and regular (no slot) microring resonator devices

a Air-cladding  
b PMMA-cladding  
Straight lines are linear fitting [19]

**Silicon photonics in communications:** As in the computing applications, silicon photonics can also play a significant role in optical communication systems. Commercial companies like Luxtera and Kotura addressing this space using silicon photonics have already started several years ago. Silicon photonics expects to potentially solve two main problems in optical communications. Two typical optical communication systems are one that heavily relies on electronic memory and processing with extremely power hungry system interfaces, and the other that heavily relies on an ‘all-optical’ data plane that lacks essential monitoring and control plane functions [25]. The first example is high capacity routers such as Cisco’s CRS-1 router, which consume nearly 1 MW at 46 Tbit/s switching capacity [26]. Memory and processors will conduct full IP (Internet protocol) functions at the line rate for every bit, even though only control plane information needs to be processed. The second example is optical add–drop multiplexers that will require separate out-of-plane signalling since the ‘all-optical’ data plane lacks intelligence. Silicon photonics can potentially bridge this gap by providing integrated electronics and optics on the same platform. Future high-capacity routers may exploit all-optical label switching [25] that utilises silicon photonics to electronically process labels after RF-photonics extraction and re-insertion and to all-optically switch the data. Potential improvement in energy efficiency exceeds 5000-fold when compared to today’s state of the art [25].

**Silicon photonic building blocks:** The building blocks for such silicon photonic EPIC systems include modulators, waveguides, multiplexers/demultiplexers, plasmonic interfaces, light sources and detectors.

**Optical modulators:** Silicon has a cubic lattice structure and there is no electro-optical (Pockel’s) effect available. Cornell, IBM and Intel have exploited the free-carrier plasma effect due to injected electrons and holes to create injection-current induced electro-optical modulation of both the real and imaginary parts of the refractive index. Normally the recombination process determines the highest speed attainable in such modulators, but carrier sweep-out in the reverse-biased depletion modulation to achieve faster than the carrier lifetime [27] and as high as 10–40 Gbit/s modulation speed [28, 29]. The Stanford group has demonstrated an Si-based electroabsorption modulator that uses the quantum-confined Stark effect within a stack of compressive Ge quantum wells separated by tensile SiGe barriers [30]. Electrical-field induced absorption of  $\Delta\alpha = 2800\text{ cm}^{-1}$  at 3 V bias has been achieved at 1438 nm wavelength [30].

**Demux/muxes:** Typical arrayed waveguide gratings (AWGs) [31] and Echelle gratings [32] ( $> 1 \times 1\text{ mm}$ ) are relatively too large to be cost effective on a CMOS platform. Instead, in essence, it is possible to utilise a series of microring resonators to multiplex and demultiplex signals; however, one must be careful of crosstalk accumulation in the signal. Very compact ( $8.2 \times 13.3\ \mu\text{m}$ ) mode demux/mux can be realised by aperiodically placed photonic structures [33] and similar devices for spectral demux/mux are also conceivable.

**Lasers:** A room temperature silicon laser by direct electrical current injection remains as an unattained goal. However, most applications do not require on-chip lasers, but rather can benefit equally or even more from external lasers because of the finite wall-plug efficiency of lasers. For instance, low-threshold lasers will have low wall-plug efficiency such that most of the pump energy will turn into heating

the chip. Keeping the light source off chip and externally modulating this light after coupling into the chip remains relatively more practical at this point.

As in InGaAsP/InP lasers, silicon-based lasers can contain layers of SiGe/Si in the active region. While silicon is an indirect bandgap material, germanium is nearly a direct bandgap material. Hence, a quantum well structure with a Ge well and a SiGe barrier is potentially a strong candidate for realising a room-temperature electrically pumped group IV laser diode operating at, or near, the fibre-optic communications wavelengths.

Silicon Raman lasers, developed by UCLA [34] and Intel [35] offered the first on-chip coherent optical source on silicon. While the silicon Raman lasers required external pump lasers and showed poor wall-plug efficiency, they provided full integrateability and tenability.

Hybrid integration of III-V laser diodes on silicon will be a cost-effective solution for on-chip light sources. Intel/University of California Santa Barbara have demonstrated [36] evanescently coupled hybrid integrated AlInGaAs-Si lasers by wafer bonding the AlInGaAs/InP active region on silicon. The relatively low bonding temperature ( $\sim 300$  K) makes it attractive for potential compatibility with CMOS processes.

**Detectors:** Germanium or GeSi on Si provides detection of optical signals at 1.3–1.5  $\mu\text{m}$ . Ge or GeSi can be deposited by chemical vapour deposition (CVD); however, the lattice constant of Ge is 4% larger than that of Si. The strain often creates dislocation defects that increase the leakage current. Ge does not form a stable oxide and lack of a passivation layer for Ge also makes it difficult to achieve a low dark current. Recently, Luxtera has demonstrated a Ge-enabled SOI-CMOS process [37] at Freescale Foundry and very recently the Intel-UCSB team has demonstrated a 340 GHz gain–bandwidth Ge–Si avalanche photodiode using CVD growth of Ge and Si layers at 850°C [38]. An alternative to high-temperature CVD is to attempt low-temperature CVD (sacrifice quality) or to conduct wafer bonding of Ge or InGaAs detector material on silicon, similarly to the way a hybrid laser was prepared.

**Plasmonics:** Collective oscillations of free electron gas (plasma) coupled with optical oscillation allow light to propagate along a surface in the form of collective electron motions. Plasmonics bridge optics with electronics, and allows extreme light localisation and coupling from dielectric photonics (SOI waveguide based) to plasmonic devices. This is potentially of significant utility since typical optical waveguide dimensions are  $\sim 300$  nm and the electronics is already down to 32 nm dimensions. Silicon photonics find aluminium rather than copper to be a better metal to provide lower loss plasmonic waveguiding. Ironically, silicon CMOS industry has discarded aluminium for copper metal lines in recent years.

**Optical isolators:** As in any photonic integrated circuits, lack of optical isolator technologies readily integrateable with silicon photonic chips is likely to be a serious roadblock in practical implementation of large scale integration. Static optical isolation [39] as well as dynamic optical isolation [40, 41] techniques are being considered for silicon photonics, and the technologies are not yet mature enough for practical implementations today.

**CMOS-compatibility:** Silicon photonic fabrication process requiring waveguide patterning, (dry) etching, metallisation, ion implantation, annealing etc. is a subset of the standard CMOS process. For this reason, silicon photonics is often hastily referred to as CMOS photonics. The actual CMOS fabrication processes used at commercial foundries typically have different process parameters (e.g. etch depth) than are desired for silicon photonics, and silicon photonics uses substrates with far thicker silicon and buried oxide layers than for CMOS electronics. Typical silicon photonics require only 5–6 mask layers and standard CMOS processes use  $\sim 40$  mask layers. Typical optical components (modulators, lasers etc.) typically occupy 10–1000  $\mu\text{m}$  lateral dimensions, and electronic components are tens of nanometres. While it is clear that there will be significant added values in silicon EPICs, market-driven philosophy may keep silicon EICs and PICs separate for a foreseeable timeframe. This may be similar to the reason why DRAMs and CPUs are still built and packaged separately today even though their integration [42] can significantly ease the latency and bandwidth bottleneck.

**Conclusions:** Silicon photonics exploits a superior material platform for photonic integration readily integrateable with large-scale CMOS electronic integrated circuits. Recent progress has been remarkable in realising the necessary component technologies on this new photonic platform. High yield, uniform and high-quality process backed by the billion dollar CMOS industry is likely to boost this technology to a new platform for next generation systems on a chip including highly functional EPICs in the future. To reach that point, significant challenges related to compatibility and practicality must be overcome.

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